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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,594	03/23/2001	Yasuhiro Yoshida	55707(904)	7185

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EXAMINER	
GOOD JOHNSON, MOTILEWA	
ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/815,594	Applicant(s) YOSHIDA ET AL.	
	Examiner Motilewa A. Good-Johnson	Art Unit 2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2, 4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is responsive to the following communications: Application, filed 03/23/2001; IDS, paper #2, filed 06/07/2001; IDS, paper #4, filed 04/15/2003.

2. Claims 1-16 are pending in this application. Claims 1, 10, 11 and 16 are independent claims. No claims have yet been amended.

3. The present title of this application is "Image Processing Apparatus and Image Display Apparatus Using Same" (as originally filed)

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Double Patenting

5. Applicant is advised that should claim 1 be found allowable, claim 11 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

6. Applicant is advised that should claim 10 be found allowable, claim 16 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content

that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-16 rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto, U.S. Patent Number 6,343,147 B1, "Print Preview and Setting Background Color in Accordance with a Gamma Value, Color Temperature and Illumination Types", class 382/167, 01/29/2002, filed 11/03/1997.

As per independent claim 1, an image processing apparatus, comprising: a first signal processing circuit for applying gamma correction to an n-bit . . . digital signal inputted as a video signal, and for converting the digital signal into an m-bit . . . digital signal; (Yamamoto discloses in figure 11, a gamma correction circuit for correction the nonlinearity of a display device, col. 11, lines 1-16, see also figure 11-15) and a second signal processing circuit for adding a noise

signal to the m-bit digital signal from said first signal processing circuit, and for outputting a Q-bit . . . digital signal obtained from rounding off a less significant m-Q bit from the m-bit digital signal. (Yamamoto discloses a noise superposing circuit in figure 11, col. 11, lines 1-17, see also figures 11-15)

With respect to dependent claim 2, first signal processing circuit includes bit-converting means for converting the inputted n-bit digital signal into the m-bit digital signal in accordance with a pre-set value. (Yamamoto discloses a matrix conversion circuit for adjusting the color tone of the input image signal, col. 11, lines 1-17, see also figures 11-15)

With respect to dependent claim 3, bit-converting means is a look up table, which outputs the m-bit digital signal that is the present value in accordance with the inputted n-bit digital signal. (Yamamoto discloses the log conversion circuit comprising a LUT, col. 4, lines 44-45)

With respect to dependent claim 4, said bit converting means is a calculating device for converting the n-bit digital signal into the m-bit . . . digital signal by numerical calculation. (Yamamoto discloses an inverse masking circuit that implements the inverse conversion and an inverse masking calculation, col. 13, lines 7-55)

With respect to dependent claim 5, said first signal processing circuit and said second signal processing circuit are provided for respective RGB colors. (Yamamoto discloses the image is captured as a RGB digital signal into the image processing apparatus via the image input circuit, col. 11, lines 22-25)

With respect to dependent claim 6, and average value of a signal level of the noise signal is set to zero. (Yamamoto discloses assuming a value between f (i-1) and f (i), col. 12, lines 1-17, superposes the noise component)

With respect to dependent claim 7, the noise signal is a random noise signal with no regularity in its cycle of amplitude. (Yamamoto discloses noise superposed on the gamma correction values is forcibly randomly distributed within a predetermined range, col. 11, lines 61-65)

With respect to dependent claim 8, the noise signal is obtained from, by using an arbitrary noise pattern table, switching a starting point of the noise pattern table per field or per noise pattern table. (Yamamoto discloses the random number generated in units of pixels, i.e. a pattern, to superpose a noise component, col. 11, lines 61-67)

With respect to dependent claim 9, a histogram of an amplitude of the noise signal shows Gaussian dispersion where zero amplitude of the noise signal is at the center. (Yamamoto discloses the random number have a Gaussian distribution, col. 14, lines 31-39)

As per independent claim 10, an image processing apparatus, comprising: a signal processing circuit for adding a noise signal to an inputted m-bit . . . digital signal, and for outputting a Q-bit . . . digital signal obtained from rounding off a less significant . . . bit . . . from the m-bit digital signal. (Yamamoto discloses superposing a noise component on a pixel value after gamma correction and converting a decimal into an integer by rounding off, col. 12, lines 10-25)

As per independent claim 11, an image display apparatus comprising a display means for displaying an image, and driving means for driving the display means . . . , it is rejected based upon similar rational as above independent claim 1.

With respect to dependent claim 12, it is rejected based upon similar rational as above dependent claim 2.

With respect to dependent claim 13, the pre-set value in said bit converting means is rewritable so that unevenness in properties of said driving means may be absorbed. (Yamamoto discloses implementing inversion conversion of the masking/ under color removal circuit, col. 13, lines 7-11)

With respect to dependent claim 14, the pre-set value in said bit converting means is rewritten in accordance with brightness in surroundings of said image display apparatus. (Yamamoto discloses the nonlinearity of the display device is correction by the correction circuit and the measured values of the monitor is distributed within the range, col. 13, line 64 – col. 14, line 7)

With respect to dependent claim 15, the pre-set value in said bit converting means is rewritten in accordance with brightness of overall display image of said display means. (Yamamoto discloses the nonlinearity of the display device is correction by the correction circuit and the measured values of the monitor is distributed within the range, col. 13, line 64 – col. 14, line 7)

As per independent claim 16, it is rejected based upon similar rational as above independent claim 10.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

2001/0008429 A1 Arimizu 348/674 07/19/2001 01/17/2001

Gamma correction circuit for imaging signal and display apparatus including such gamma correction circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Motilewa A. Good-Johnson whose telephone number is (703) 305-3939. The examiner can normally be reached on Monday - Friday 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-0377.

Motilewa Good-Johnson

Motilewa A. Good-Johnson
Examiner
Art Unit 2672

mgj